

Comparison of Switching Methods for Asymmetric Cascaded H-Bridge Multilevel Inverter

Mohammad Soltani¹, Mohammad Hosein khazade²

¹(Department of Power Electrical Engineering, Iran university of science and technology, Tehran, Iran)

²(Department of FAVA Engineering, Imam Hosein University, Tehran, Iran)

Abstract: - Recently, multilevel inverters using for medium voltage drive are controlled with various modulation techniques. Although we have seen in Asymmetric Cascaded H-Bridge topologies having unequal input dc voltages significant improvement than others, its switching is complex. In this study all three applicable methods on Asymmetric CHB, SHE, NLC and Multi-carrier, are analyzed. In multi-carrier switching method for this topology the number of subject switches is less than carriers. We introduce equations for combine the PWMs to use the controllability advantage of the multi-carrier method in asymmetric topology. Comparing these methods shows although the SHE and NLC have lower THD; they are Off-Line methods and are not applicant for closed-loop systems. Finally, results indicate that multi-carrier method has an appropriate harmonic function and has advantage rather than two other switching methods for asymmetric multi-level inverter respect to its Online nature.

Keywords: - Multilevel inverter, Asymmetric CHB, combined PWM, THD.

I. INTRODUCTION

In recent years, there is a growing demand for high-power applications while capable of providing high output voltage signals and having good spectral performance and easy control. To overcome the limitations of semiconductor voltage and current rating, it is necessary to parallel or series connection between converter cells [1]-[4]. Multi-level inverters have been attended, because their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages. However, the increasing number of devices tends to reduce the overall reliability and efficiency of the power converter [5]. They have many attractive features like high voltage capability, reduced common mode voltages, low switching losses, high voltage capability, near sinusoidal outputs and smaller or even no output filter, making them suitable for high power applications[5]-[8]. They synthesize an output voltage waveform from several levels of dc voltage sources. As the number of levels increases, the combined output waveform approaches the sinusoidal wave with the reduced harmonic distortion [6]. The well-known circuit topologies are: cascaded H-bridge multi-level inverter [9]-[13], diode-clamped multi-level inverter [14] and flying-capacitor multi-level inverter [15]. However each inverter topology is having its own advantages and disadvantages. These topologies can be combined together, to have output multilevel voltage with lower switching loss, lower THD and regenerative advantages.

They are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: level shifted and phase shifted [14]. Other established modulation methods include the multi-level extension of space vector modulation (SVM), multi-level selective harmonic elimination (SHE) [16]-[19] and nearest level control (NLC) [20]-[22]. The last three methods are used for lower switching frequency applications.

The CHB topology of multi-level inverter can be in two topologies include symmetric and asymmetric. The symmetric multi-level inverters have the same voltage on each of dc input. The asymmetric multi-level inverters have similar circuit topology as symmetric multi-level inverters. They differ only in the input dc voltages and switching procedure. Higher output quality can be obtained with smaller circuit and control complexity [23], [24]. The essential discussion regarding CHB topology involves the cost and the volume of the facilities. The need for more dc sources is a drawback in the CHB [14]. Using unequal dc sources for each cell removes this drawback to a certain degree and reduces the number of switches. The volume of transformer reduction for geometry input dc voltages to the cells in the network applying the whole voltage capacity of the switches for unit with high voltage, a reduction in the number of regenerative facilities to the network upon need, reduction switching loss and etc. [7].

In asymmetric CHB power injection and uniform switching properties of the cells are eliminated while, the number of the cells applied in forming multi-level output voltage decrease significantly. To have the highest number of output voltage levels in asymmetric CHB the proportion between dc voltage sources of the cells must be 3^n [20]. An asymmetric 9-level is illustrated in Fig. 1. Switching the inverters of CHB series is usually conducted through SHE and multi-carrier methods. In the asymmetric CHB series, the adopted methods are of SHE and NLC through obtaining the switching angles with less concern on multi-carrier method; since, in the

method the number of switches is not of major concern, while, merely the output voltage and its harmonics are of concern. The method, through simple is off-line and is non-efficient in closed-loop system.

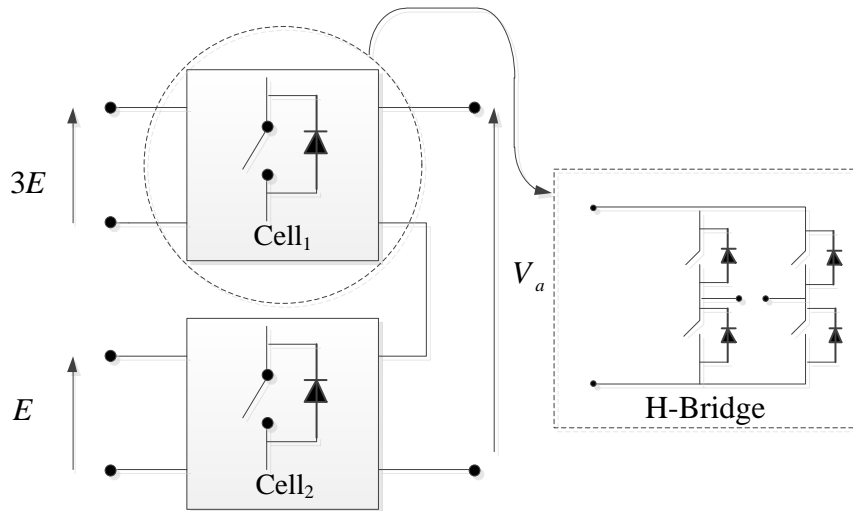


Fig. 1- The 9-level asymmetric CHB

II. SWITCHING ALGORITHM FOR ASYMMETRIC CHB

a. SHE

The advantages of SHE method are the lowest value of THD and switching loss. Because of modularity and simply In CHB topology, this method is considered. In this method, state of any switches just once is ON and OFF in any cycle. In this case, switching angles can be achieved with the minimum THD.

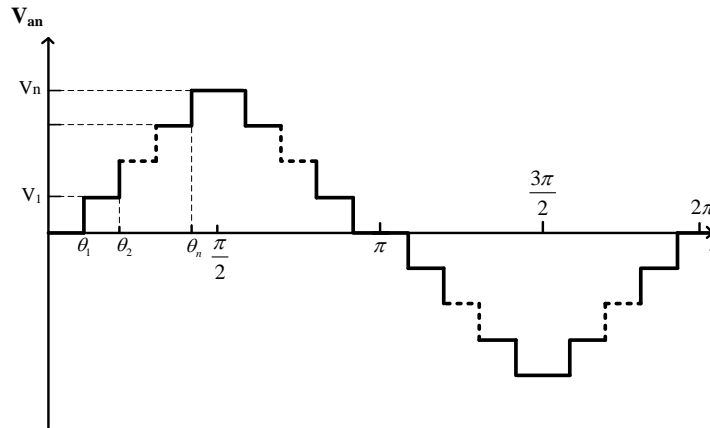


Fig. 2- The staircase output of (2n+)-level inverter

One of the multilevel inverter issues is harmonic order, while can be measured by different methods. Fig. 2 shows a staircase voltage waveform synthesized by a (2N + 1) level converter. Using the Fourier series, the staircase multilevel voltage waveform of Fig. 2 is expressed by [18]

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\alpha) \tag{1}$$

Where V_n represents the amplitude of the harmonic of order n and is expressed by

$$V_n = \frac{aV_{dc}}{n\pi} \sum_{i=1}^N \cos(n\alpha_i), \quad n = 1, 5, 7, 11, \dots \tag{2}$$

V_{dc} is the dc voltage of each output voltage level. The switching angles $\alpha_1, \alpha_2, \dots, \alpha_n$ must satisfy the following constraint

$$0 \leq \alpha_1 \leq \alpha_2 \leq \dots \leq \alpha_n < \frac{\pi}{2} \tag{3}$$

The procedure of SHE-PWM technique is to determine the switching angles $\alpha_1, \alpha_2, \dots, \alpha_n$ and the fundamental component is adjusted to its desired amplitude, while any low order odd harmonic distortion except third harmonic are eliminated [17].

$$\begin{cases} \sum_{i=1}^N \cos(\alpha_i) = NM \\ \sum_{i=1}^N \cos(5\alpha_i) = 0 \\ \vdots \\ \sum_{i=1}^N \cos(n\alpha_i) = 0 \end{cases} \quad (4)$$

Where $n=3N-1, \dots$, when N is even, $n=3N-2, \dots$, when N is odd. M is the modulation index and is defined as

$$M = \frac{V_1}{4NV_{dc}/\pi} \quad (5)$$

To determine the switching angles, the N transcendental equations in Eq. (4) should be solved. The standard SHE method has a narrow modulation region and cannot be realized for the entire modulation range. For finding the optimized value of switching angles in minimum THD can be used from various optimization methods. One of them is Genetic Algorithm (GA). At first for have minimum THD in eq. (6), we premise the Eqs (4), (5) for obtaining optimized switching angles [19].

$$THD = \frac{\sqrt{\sum_{n \neq 1} \left(\frac{\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_L)}{n} \right)^2}}{\cos(\alpha_1) + \cos(\alpha_2) + \dots + \cos(\alpha_L)} \quad (6)$$

A GA is a learning algorithm that imitates the evolution of organisms. In the natural evolution process of organisms, the reproduction of a set of individuals that forms a certain generation is such that those individuals with fitness to environmental adaptation survive with high probability. Reproduction that is based on the degree of conformity of an individual in a GA as an artificial model that imitates the evolution process of such an organism is performed, and the next-generation population is generated through crossover and mutation. The process is carried out by repeating such genetic operations, and if the individual of the last generation that fulfills end conditions can be found, the semi-optimal solution in question may be determined. For Asymmetrical CHB inverter SHE method is purposed, although that has many drawbacks in closed-loop systems.

b. NLC

Asymmetrical CHB multilevel inverters can be modulated with nearest level control (NLC). In this method the voltage levels are chosen nearest to the reference voltage. The NLC gives an excellent output voltage quality, and it produces an inverse relationship between frequency and distributed power from each cell. Fig. 3 shows the output voltage of the 27-level inverter, which each level voltage is V_{dc} and reference voltage is passed through it. When V_{dc} is constant, the output voltage must be controlled by using PWM directly on the H-bridges. This method is one of offline method like SHE, having drawback in closed-loop. But that is very simple method to obtain the lowest level of THD [21].

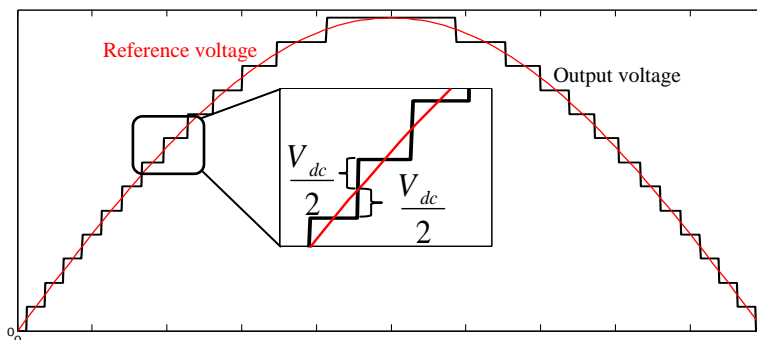


Fig. 3- The NLC method for multilevel output

c. SPWM

In level shifted switching, 27-level voltage is formed, including 27-voltage levels at above and below the coordinate access, where each requires one carrier wave. The $S_1, S_4, S'_1, S'_4, S''_1$ and S''_4 switches are directly commanded by the microcontroller and switches $S_3, S_2, S'_3, S'_2, S''_3$ and S''_2 are of their corresponding NOT state, Fig. 4. This phenomenon is due to lack of simultaneous of ON switches of one branch and avoid from possible vulnerability. The problem with switching in asymmetric CHB is that the number of separate PWM (that generated by comparing the carrier waves with the reference wave) are 26, but the number of the subject switches are 6. Overall, two PWM pulses are required for each cell, that is, these face switches function are formed by a combination of twenty six PWMs which eventually results in the output voltage in state of three cells.

The carrier waves for a 27-level inverter are illustrated in Fig. 5. According to Fig. 4, cell 3 with $+9V_{dc}$ in input voltage is an H-Bridge inverter, applied for the 3-level output voltage. Here, switching of cell1 where combined PWM generated from carriers is applied. The whole command blocks of all three cells are drawn in Fig. 4.

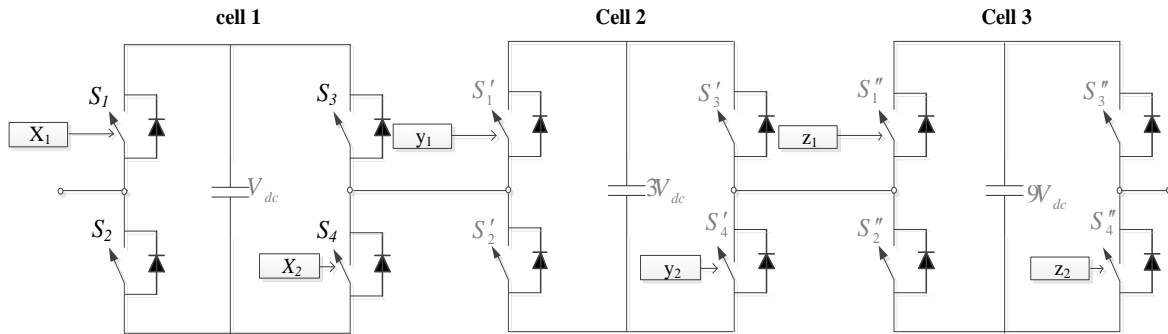


Fig. 4- The control blocks of the three inverter cells to generate 27-level output

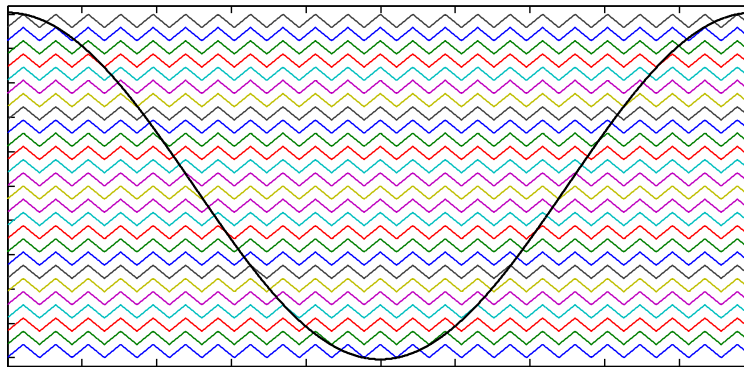


Fig. 5- The carrier waves for a 27-level inverter

In this switching, it is assumed that $S_1, S_4, S'_1, S'_4, S''_1$ and S''_4 are the subjects of the command. If the PWMs of the positive carriers in coordinate axes are named as P_1-P_{13} and the negative coordinate axes are named as q_1-q_{13} , then, the switches state to provide cell₁, cell₂ and cell₃ for different levels would be presented as tabulated in Table (1). In this table, the sign (-) denoted OFF and the sign (+) denotes ON. When the diode is in parallel and inverse position, the switch is assumed ON state. When the output voltage level reaches upper than $+V$ or less than $-V$, the output of cell₃ would be $\pm 3V_{dc}$ hence, the obtained PWM from carrier of the same level is applied to high voltage cell.

As observed in Table 1, in order for the z_1 and z_2 commands, Fig. 4, to have a 3-level voltage in cell₃, p_5 and q_5 become applicable, Eqs. (7 and 8).

$$z_1 = p_5 \tag{7}$$

$$z_2 = q_5 \tag{8}$$

To obtain the combined equation of PWMs, for the cell₂, the S'_1 in the positive coordinate axes, any change in switching situation of the PWM subject are added with respect to their signs. If in the negative coordinate the voltage levels are sought, any change in switching situation of the PWM subject are deducted that is. On the other hand, the total status change of the p_s and negative of q_s constitute the general equation for S'_1 switch through the following equation:

$$y_1 = p_2 + p_{11} + q_8 - p_5 - q_5 \tag{9}$$

To command S'_4 switch, the PWMs symmetric of switching in Eq. (9) are applied. In fact, this symmetry is the difference of 180° between S'_4 and S_1 command and the ps in Eq. (9) are converted to qs in Eq. (10) and vice versa. Therefore, the PWM control equation for the S_4 is presented as: Eq. (10). Cell₁ switching function is achieved in accordance with this procedure. These functions are according to Eqs. (11, 12)

$$y_2 = q_2 + q_{11} + p_8 - q_5 - p_5 \tag{10}$$

$$x_1 = p_1 + p_4 + p_7 + p_{10} + p_{13} + q_3 + q_6 + q_9 + q_{12} - p_2 - p_5 - p_8 - p_{11} - q_2 - q_5 - q_8 - q_{11} \tag{11}$$

$$x_2 = q_1 + q_4 + q_7 + q_{10} + q_{13} + p_3 + p_6 + p_9 + p_{12} - q_2 - q_5 - q_8 - q_{11} - p_2 - p_5 - p_8 - p_{11} \tag{12}$$

Table 1- general switching states of the 27-level output

PWM	Cell 1	S_1	S_4	Cell 2	S'_1	S'_4	Cell 3	S''_1	S''_4	Output voltage
P_{13}	$+V_{dc}$	+	+	$+3V_{dc}$	+	+	$+9V_{dc}$	+	+	$13V_{dc}$
P_{12}	0	-	+	$+3V_{dc}$	+	+	$+9V_{dc}$	+	+	$12V_{dc}$
P_{11}	$-V_{dc}$	-	-	$+3V_{dc}$	+	+	$+9V_{dc}$	+	+	$11V_{dc}$
P_{10}	$+V_{dc}$	+	+	0	-	+	$+9V_{dc}$	+	+	$10V_{dc}$
P_9	0	+	-	0	-	+	$+9V_{dc}$	+	+	$9V_{dc}$
P_8	$-V_{dc}$	-	-	0	-	+	$+9V_{dc}$	+	+	$8V_{dc}$
P_7	$+V_{dc}$	+	+	$-3V_{dc}$	-	-	$+9V_{dc}$	+	+	$7V_{dc}$
P_6	0	-	+	$-3V_{dc}$	-	-	$+9V_{dc}$	+	+	$6V_{dc}$
P_5	$-V_{dc}$	-	-	$-3V_{dc}$	-	-	$+9V_{dc}$	+	+	$5V_{dc}$
P_4	$+V_{dc}$	+	+	$+3V_{dc}$	+	+	0	-	+	$4V_{dc}$
P_3	0	+	-	$+3V_{dc}$	+	+	0	-	+	$3V_{dc}$
P_2	$-V_{dc}$	-	-	$+3V_{dc}$	+	+	0	-	+	$2V_{dc}$
P_1	$+V_{dc}$	+	+	0	+	-	0	-	+	V_{dc}
0	0	-	+	0	+	-	0	-	+	0
q_1	$-V_{dc}$	-	-	0	+	-	0	-	+	$-V_{dc}$
q_2	$+V_{dc}$	+	+	$-3V_{dc}$	-	-	0	-	+	$-2V_{dc}$
q_3	0	+	-	$-3V_{dc}$	-	-	0	-	+	$-3V_{dc}$
q_4	$-V_{dc}$	-	-	$-3V_{dc}$	-	-	0	-	+	$-4V_{dc}$
q_5	$+V_{dc}$	+	+	$+3V_{dc}$	+	+	$-9V_{dc}$	-	-	$-5V_{dc}$
q_6	0	-	+	$+3V_{dc}$	+	+	$-9V_{dc}$	-	-	$-6V_{dc}$
q_7	$-V_{dc}$	-	-	$+3V_{dc}$	+	+	$-9V_{dc}$	-	-	$-7V_{dc}$
q_8	$+V_{dc}$	+	+	0	-	+	$-9V_{dc}$	-	-	$-8V_{dc}$
q_9	0	+	-	0	-	+	$-9V_{dc}$	-	-	$-9V_{dc}$
q_{10}	$-V_{dc}$	-	-	0	-	+	$-9V_{dc}$	-	-	$-10V_{dc}$
q_{11}	$+V_{dc}$	+	+	$-3V_{dc}$	-	-	$-9V_{dc}$	-	-	$-11V_{dc}$
q_{12}	0	-	+	$-3V_{dc}$	-	-	$-9V_{dc}$	-	-	$-12V_{dc}$
q_{13}	$-V_{dc}$	-	-	$-3V_{dc}$	-	-	$-9V_{dc}$	-	-	$-13V_{dc}$

III. SIMULATION RESULTS

The first paragraph under each heading or subheading should be flush left, and subsequent paragraphs should have a five-space indentation. A colon is inserted before an equation is presented, but there is no punctuation following the equation. All equations are numbered and referred to in the text solely by a number enclosed in a round bracket (i.e., (3) reads as "equation 3"). Ensure that any miscellaneous numbering system you use in your paper cannot be confused with a reference [4] or an equation (3) designation. In the simulation, we perform on the 27-level inverter each of the three methods, SHE, NLC and SPWM. The input dc voltage in cell1 is 30v. In SHE method for optimization the amount of THD is used from GA; such that, Eq. (4) is satisfied and Eq. (6) is the lowest. The switching angles obtained from theoretical THD and simulated THD are tabulated

in table (2); fitness value of GA for finding the best value of THD in its statistics society shows in Fig. (6); the output 27-level voltage and its harmonic orders switched by SHE method in Simulink illustrate in Fig. 7. The simulation result is very close to theoretical THD.

Table 2- The simulation and theoretical THD with switching angles (degree) obtained from GA

θ_{13}	θ_{12}	θ_{11}	θ_{10}	θ_9	θ_8	θ_7	θ_6	θ_5	θ_4	θ_3	θ_2	θ_1	Theoretical THD (%)	Simulation THD (%)
71.6	61.3	52.5	46.1	40.2	35.1	29.5	24.3	20.1	15.5	11.1	6.87	2.29	2.928	2.98

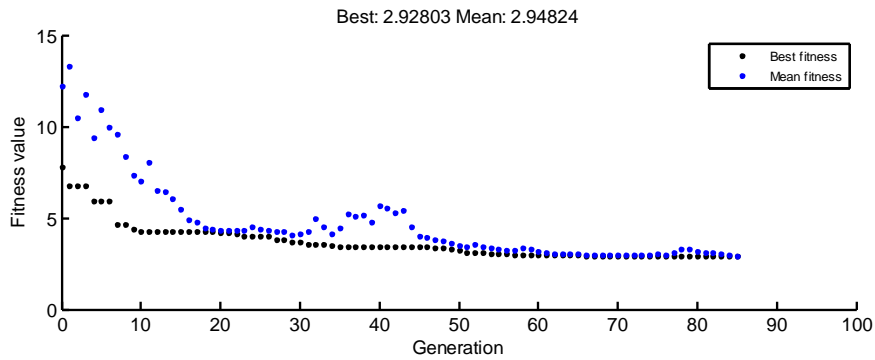


Fig. 6- Fitness values of GA for finding THD

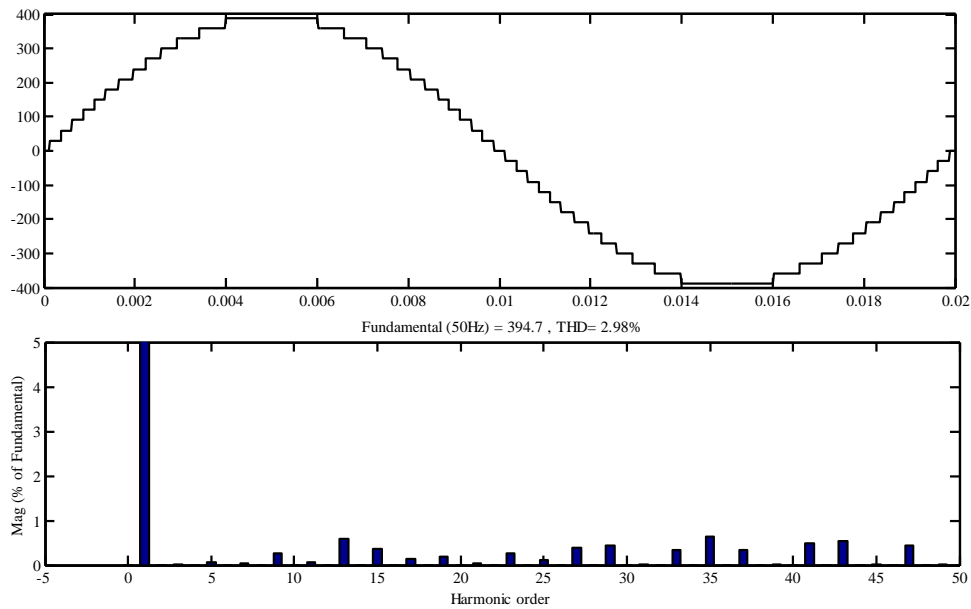


Fig 7- The output 27-level voltage and its harmonic orders switched by SHE method

The voltage levels are chosen nearest to the reference voltage for implementation of NLC method on 27-level asymmetric CHB. Output voltage of each cell in test system, output of 27-level inverter switched with this method and its harmonic orders illustrate in Fig. 8.

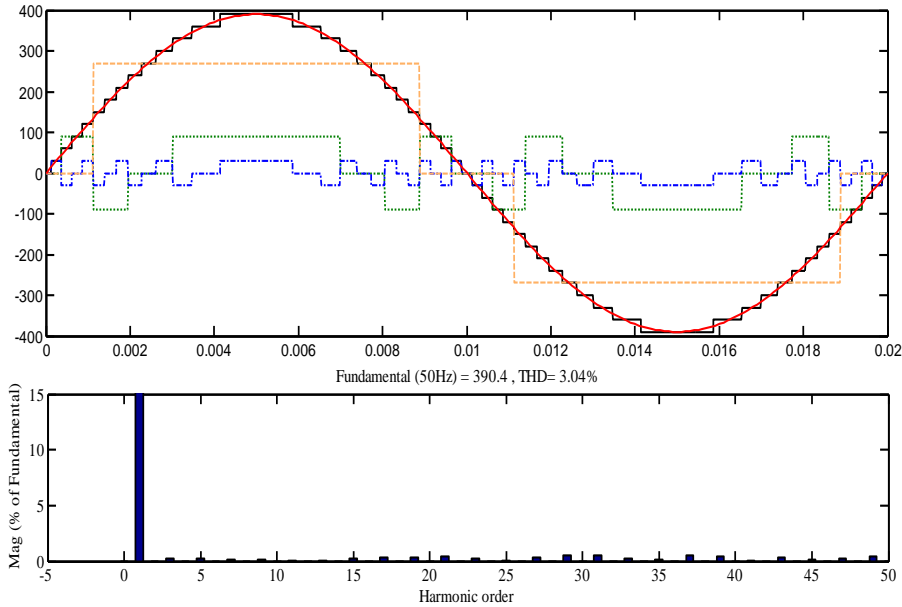


Fig 8- The output 27-level voltage and its harmonic orders switched by NLC

When carrier waves in Fig. 5 are implemented on 27-level inverter (Fig. 4) and PWMs are combined within Eqs. (7-12), we have 27-level voltage in output. This phenomenon in multi-carrier method is the opposite and as observed in Fig. 9, the best function of THD when the ma close to one and the mf is odd. The volumes of the modulation and frequency indexes applied in the previous simulation are illustrated in Fig. 9. The 27-level output voltage in the best condition found from Fig. 9 illustrate in Fig.10; switching frequency is 1150 and modulation index is 1.03. Obviously, the first harmonic distortion falls on 23 and output THD is close to 4%. The multicarrier method has an acceptable range of THD (less than 5%); although have worse result in compare two other methods. This method is online and by changing reference wave can be used for closed-loop systems. But SHE and NLC are offline method and they're not applicable for these systems.

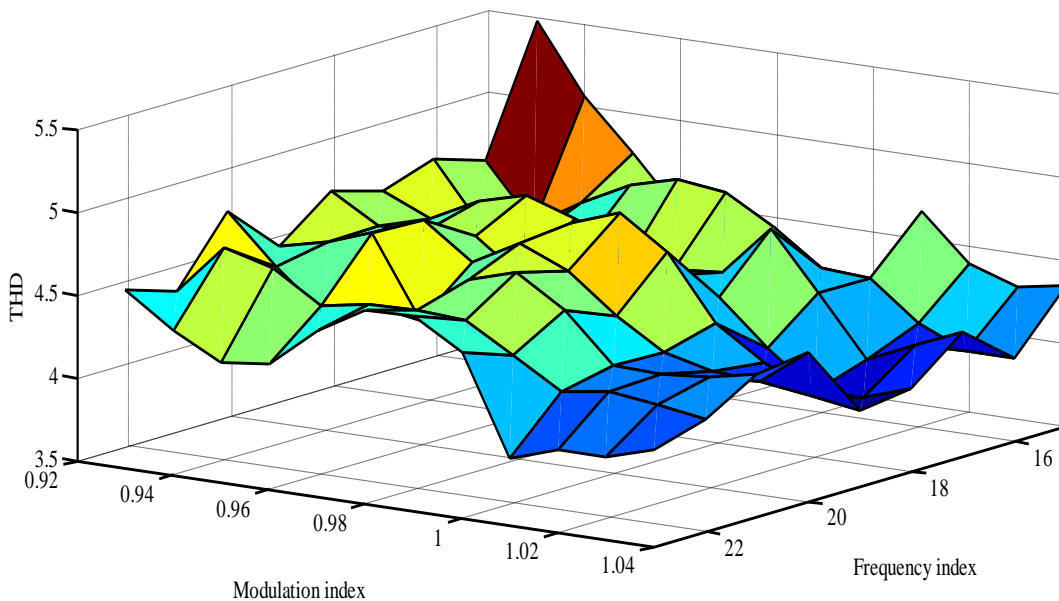


Fig 9- Comparison of output voltage THD at different m_f per m_a in SPWM

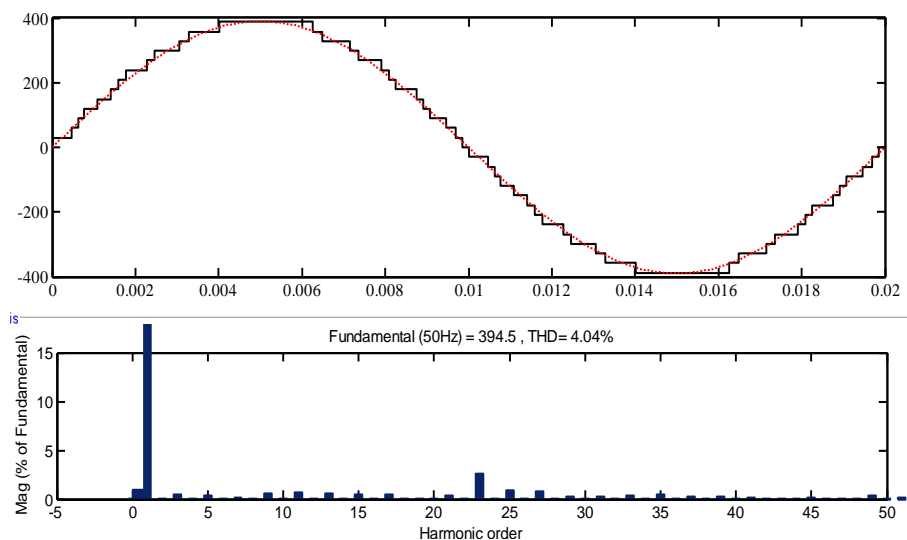


Fig 9-The output voltage of 27-level and its harmonic components in SPWM method

IV. CONCLUSION

A conclusion section must be included and should indicate clearly the advantages, limitations, and possible applications of the paper. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

In asymmetric CHB topology the number of the applied inverter units in forming multi-level voltage decreases significantly. The switching method of this topology becomes complicated due to a reduction in the subject switch count. Result shows that although The SHE and NLC methods have the best THD for staircase output voltage closed to 3% in 27-level inverter, they are Off-Line method; they're not applicable for closed-loop systems. In multi-carrier method for this topology the number of carriers is more than the subject switches. Combined PWM method is proposed to make the multi-level output voltage for asymmetric inverter efficient in medium voltage drives. Results indicate that this approach has an appropriate harmonic function and respect to its Online nature it is advantages to two other switching method for asymmetric multi-level inverter.

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